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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,898	03/30/2004	Motoki Kanamori	XA-10067	1325

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,898	KANAMORI ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Preliminary Amendment filed on March 30, 2004. Claims 11-14 been canceled. Claims 9 and 10 have been amended. Claims 1-10 are presented for examination. Claims 1-10 are pending.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in April 25, 2003 on Japanese Application No. 2003-121388. It is noted, however, that applicant has not filed a certified copy of said application as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 states, "the controller controls a first data output timing that satisfies the first operation standard and the second operation standard". However, there is nowhere in the specification disclosed a first data output timing that satisfies the first

operation standard (MMC standard) and the second operation standard (SD standard). In contrast with what is being claimed, Fig. 25 and Fig. 26 and their corresponding descriptions on page 9 shows two different data output timings, one for SD standard (second standard) and the other for MMC standard (first standard). Therefore, claim 1 is not claiming what is being disclosed in the disclosure.

Claim 1 further states, "controller controls a first data output timing that satisfies the first operation standard and the second operation standard in a first operation mode". The subject matter being claimed in claim 1 is not the same as what being disclosed in the Specification because the Specification disclosed a multimedia card (first operation standard) operates in the two operation modes, namely, the MMC mode (first operation mode) being the normal operation mode and the HS-MMC mode (second operation mode) being the next-generation standard, which operate faster than the MMC mode (see page 11, last paragraph to page 12 of the Specification). There is nowhere in the Specification discloses a first operation mode (MMC mode) that operates in a first operation standard (MMC standard) and a second operation standard (SD standard).

Further review of the specification in page 40, last paragraph to page 42 shows that the invention is to provide a memory card that can be used on the host conforming to the SD card, while achieving the conformity to both standards of the MMC mode and the HS-MMC mode. It further clarifies the invention in page 41, indentation (1) by stating that a memory card conforms to both of the modes of the first operation mode (MMC mode) and the second operation mode (HS-MMC mode) in the first operation

standard (MMC standard), while securing the compatibility of the first operation standard (MMC standard) and the second operation (SD standard).

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6, it is unclear how "a data output timing switching unit that switches a rise time/fall time **of the data** in the first data output timing". The specification does not disclose how a rise time/fall time of the data is being switched while it is not readily familiar by one having an ordinary skill in the art.

All dependent claims are rejected as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 2, 4, 6, and 7 are rejected under 35 U.S.C. 102(a) as being anticipated by Kawai et al. (2003/0090953).

As per claim1, Kawai et al. discloses a memory card conforming to a first operation standard and a second operation standard, comprising:

a non-volatile semiconductor memory having plural semiconductor memory cells, capable of storing given information, and a controller that executes operation instructions to the non-volatile semiconductor memory on the basis of commands issued from the outside (page 4, paragraph 0043), wherein:

the controller controls a first data output timing (output clock, page 2, paragraph 0012, line 13) that satisfies the first operation standard (page 1, paragraph 0003, lines 6-13, wherein each standard corresponding to each mode) and the second operation standard (see page 2, paragraph 0012, lines 28-30, operating in adjusted timing), in a first operation mode[[,]]; and

the controller controls a second data output timing (adjusted output timing, see page 2, paragraph 0012, lines 28-30) that satisfies the second operation standard, in a second operation mode (high-speed mode, page 2, paragraph 0012, lines 17-20).

As per claim 2, Kawai et al. discloses a memory card, wherein:

the controller includes a data timing switching unit that outputs data at a fall edge of a clock signal in the first data output timing, and outputs data at a rise edge of a clock signal in the second data output timing (page 5, paragraph 0059, wherein data timing switching unit is an inherent feature of Kawai et al. since a clock signal has to alternate from fall edge to rise edge and so on).

As per claim 4, Kawai et al. discloses a memory card, wherein:

the controller includes a timing delay switching unit (Fig. 1, item 10, timing adjusting circuit) that outputs data at a first delay time at the first data output timing, and outputs the data at a second delay time being shorter than the first delay time at the second data output timing (page 5, paragraph 0058, wherein the clock is delayed to synchronize with the data output therefore one of the delayed time is shorter than the other delayed time).

As per claim 6, Kawai et al. discloses a memory card, wherein:

the controller includes a data output time switching unit that switches a rise time/fall time of the data in the first data output timing, so that the rise time/fall time of the data becomes shorter to the first data output timing (see page 5, paragraph 0058-0059, wherein the clock is delayed/switched to synchronize with the data output timing).

As per claim 7, Kawai et al. discloses a memory card, wherein the data output time switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set (See Fig. 10 and corresponding figure description on page 4 paragraph 0051, wherein the output clock signal/timing is set by plurality of delayed clock);

an output buffer (Fig. 1, item 9) that outputs data on the basis of an output data enable signal (Fig. 6, item 403, dat_oe_0-3), when one of the first data output timing and the second data output timing is set to the timing register (page 4, paragraph 0051, and Fig. 10, wherein the first and second data output timing is set at the time adjusting circuitry),

an auxiliary output buffer (Fig. 6, item 26s) that outputs data on the basis of the output data enable signal (Fig. 6, item 403, dat_oe_0-3) at the second data output timing, and

an auxiliary output buffer enable unit that outputs the output data enable signal to the auxiliary output buffer, when the second data output timing is set to the timing register. See page 6, paragraph 0066 and Fig. 6 and 10, wherein the data is output at its output timing as the time the output enable signal is enabled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. (2003/0090953) in view of Yagishita (2002/0145935 A1).

As per claim 10, Kawai et al. disclosed non-volatile semiconductor memory (flash memory, Fig. 1, item 2, page 4, paragraph 0043, lines 2-3).

Kawai et al. did not specifically disclose a controller controls the plural non-volatile semiconductor memories arbitrarily in parallel operation in correspondence with the parameter value set to the power consumption parameter register.

Yagishita disclosed a power consumption and operation frequency in a circuitry wherein the lowering the operation frequency will reduce the power consumption; hence, they are operating in parallel (See Abstract, lines 11-12; and page 1, paragraph 0010, lines 6-13). Power consumption parameter register is readily apparent to one having an ordinary skill in the art since a register to hold the power consumption value is a required feature in a circuitry. Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to recognize that the power consumption is being controlled in corresponding to (or in parallel to) the

operation requirement such as the nonvolatile memories in order to supply enough of voltage and current to perform the operation without error while increasing the efficiency.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Natori (US 2003/0151070) discloses a circuit of a non-volatile semiconductor memory device wherein the power source (voltage) is gently rise corresponding to the level of the frequency of the operation mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanh Vo
Patent Examiner
Art Unit: 2189
3/28/2006

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER